
# Fibridge TDMoIP

# Datasheet

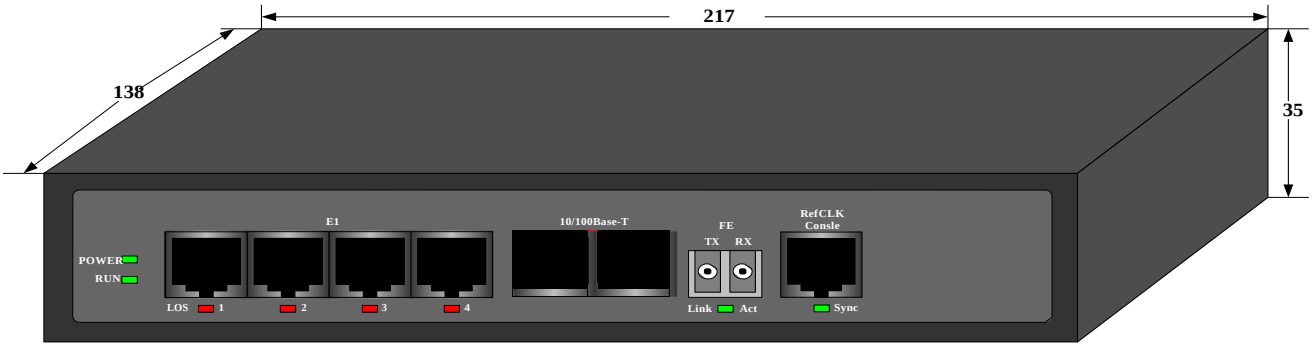
Website:
www.fibridge.com.au

# 1 Introduction

## 1.1 Brief introduction

Fibridge TDMoIP is mainly used to build telecom level E1 channel based on Ethernet/IP Network/MPLS, realize transportation in 1/2/4 channel E1 port and two local Ethernet. F5-2315/2325/2325 series TDMoIP equipment supports TDM data stream transparently transport on UDP/IPv4、MPLS and MEF network.

## 1.2 Equipment appearance and engineering parameter



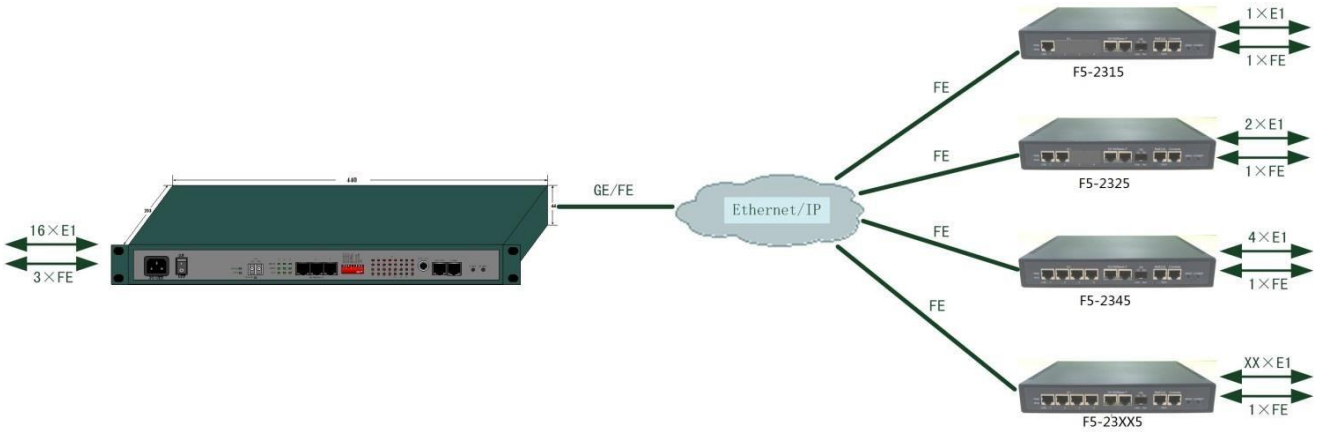

## 1.3 Main feature

- E1 port compliant with G.703, G.704 protocol, support 75ohm or 120ohm.
- E1 support CESOPSN or SATOP packing.
- Each channel E1 supports pack size 1, 2, 4, 8, 12 and 16 frame.
- Each channel E1 supports jitter buffer up to 1 ~ 256ms.
- Supports four types of clock recovery mode: auto-adapt, differential, system and loopback.
- Auto adapt clock recovery accuracy is up to 10ppb.

- TDM business compliant with IETF PWE3 protocol, support ITU-T protocol Y.1413 and Y.1453, IETF RFC4553, RFC5086, MEF-8 and MFA 8.0.0.
- Ethernet embed layer 2 switch function, supports VLAN division based on 802.1q and 802.1a, supports 802.1p protocol.
- Supports UDP/IPv4, Metro Ethernet (MEF-8) and MPLS(MFA-8) protocol.
- Supports ARP and RTP protocol.
- Supports Ethernet electrical port speed rate limit, range from 32Kbps to 100Mbps, minimum adjust unit is 32kbps.
- Supports AC220V/DC-48V power supply.

## 1.4 Typical application

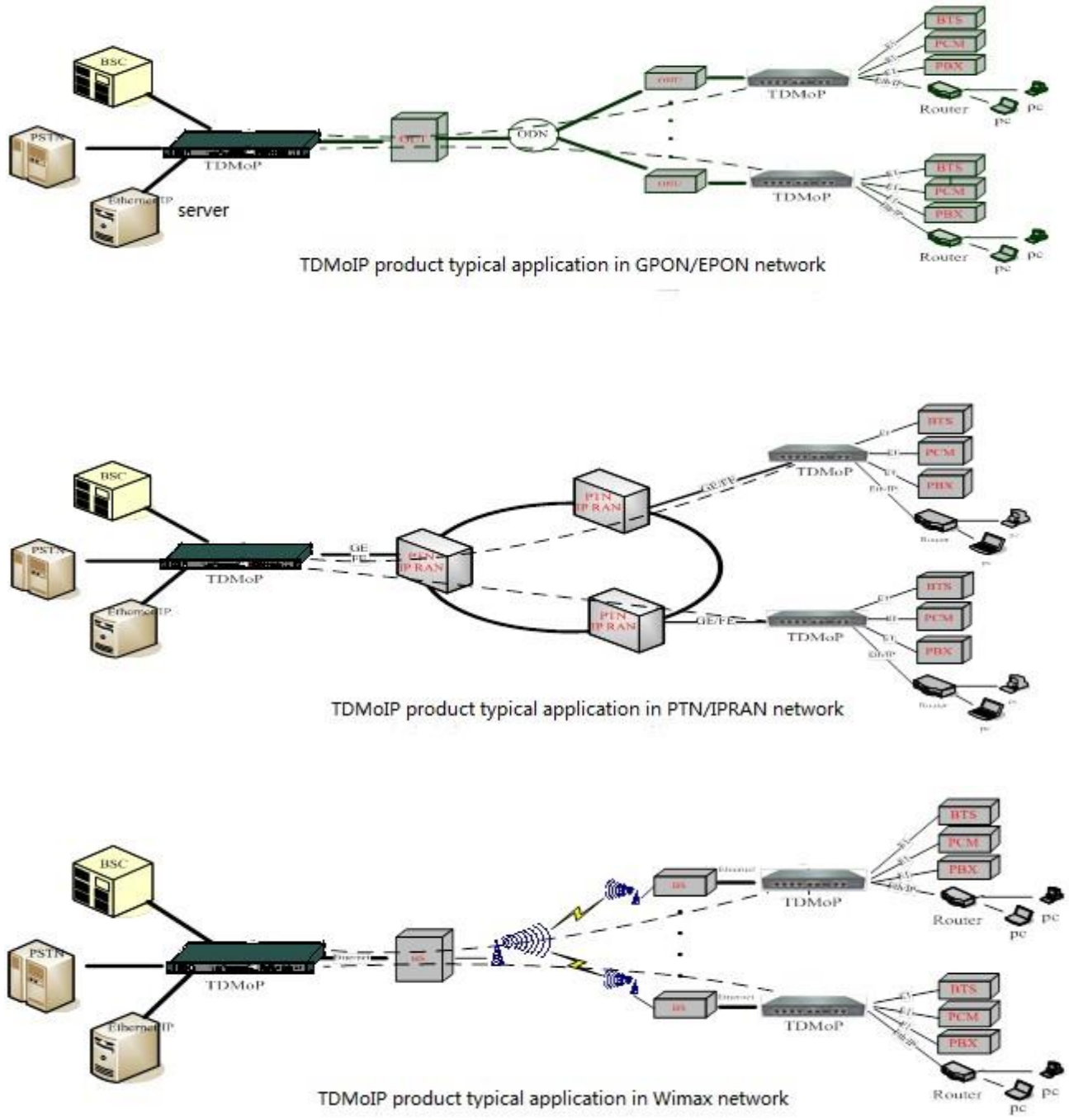
Aggregate type TDMoIP can connect with F5-2315/2325/2345, to fulfill point to multi point application, also point to point link.




Pic 1.4-1 point to multipoint application


Pic. 1.4-2 point to point application

F5-2315/2325/2345 series products can establish 1/2/4 channels transparent E1 channel on Ethernet or IP network, which is used to provide real time business like voice and images, with typical application as picture 1.4-3.




Pic.1.4-3 F5-2315/2325/2345's typical application in kinds of networks

In above topologies, F5-2315/2325/2345 can transport 1/2/4 channels E1 signal by Ethernet, connect base station controller, PSTN access network equipment and other E1 terminal equipment. Through F5-2315/2325/2345's random FE/Fx port, two locations' routers can realize local Ethernet data's mutual transmission, internal QoS system guarantees E1 signal transit's priority.

## 1.5 clock mode

F5-2315/2325/2345 provides auto-adapt, differential, system and loop back clock recovery mode.

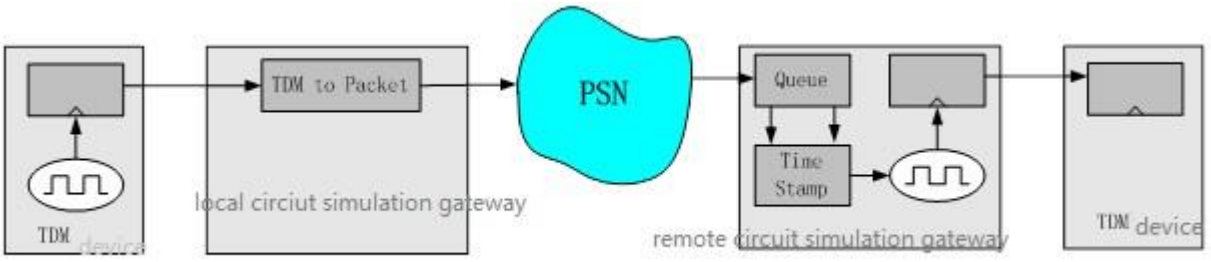
Local device and remote device clock mode configuration:

| local \ remote | Auto-adapt | differential | system | loopback |
|---|---|---|---|---|
| Auto-adapt | √ | | | √ |
| differential | | √ | | |
| system | | | √ | |
| loopback | √ | | | |

### 1.5.1 auto-adapt clock mode

Auto-adapt clock recovery mode doesn't need public clock, is easy to use, cost-effective.

F5-2315/2325/2345 gateway's auto-adapt clock recovery mode can filter most of message time delay difference; in the meanwhile raise system network adaption. E1 clock recovered from auto-adaption has little jitter, stable frequency, typical frequency shift under currency running is within ±50ppb, clock jitter less than 0.03UI.




Picture1. auto-adapt clock mode

### 1.5.2 Differential clock recovery mode

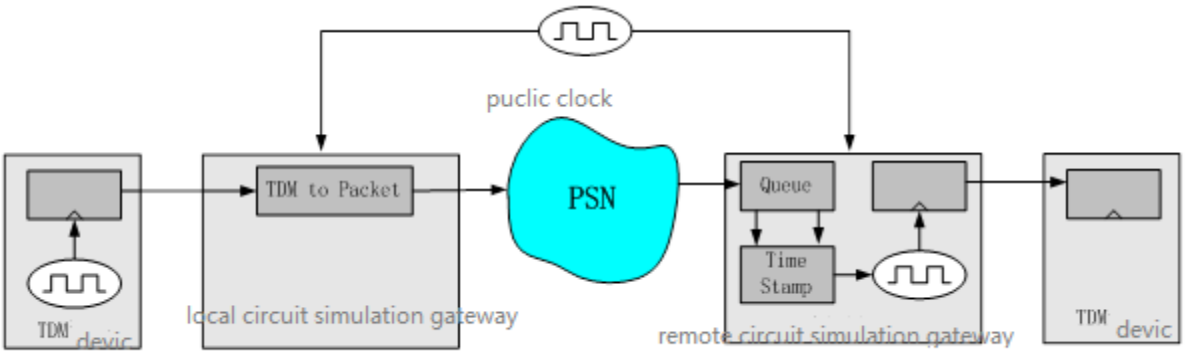
Differential clock recovery mode needs public clock comparing to auto-adapt mode. Differential clock recovery mode has highly precise recovery clock. Additionally, clock recovery is hardly impacted by PSN time

delay jitter. Therefore, Differential clock recovery mode is an ideal option under application circumstance where public clock is available.

The working theory is as follows:

The Circuit simulation gateway equipment in local site regularly sends time stamp information to remote site. This time information is provided together with RTP head and E1 simulation message. The remote site's gateway equipment abstracts time stamp from RTP head, then recovers business E1 clock through differential clock recovery algorithm.

F5-2315/2325/2345 supports differential clock recovery algorithm, through Time stamping error compensation and source highly multiplexes technology, significantly increase E1 clock recovery accuracy; and lower cost by saving FPGA source. The public reference clock supported by F5-2315/2325/2345 can be TDM clock provided by central site, or clock provided by GPS receiver. Clock frequency is 8KHz ~ 25MHz （8KHz integral multiple）. Support SDH system clock (19.44 MHz), ATM system clock (9.72 MHz or 19.44 MHz), GPS system clock(8.184 MHz) and synchronous Ethernet system clock (25 MHz).

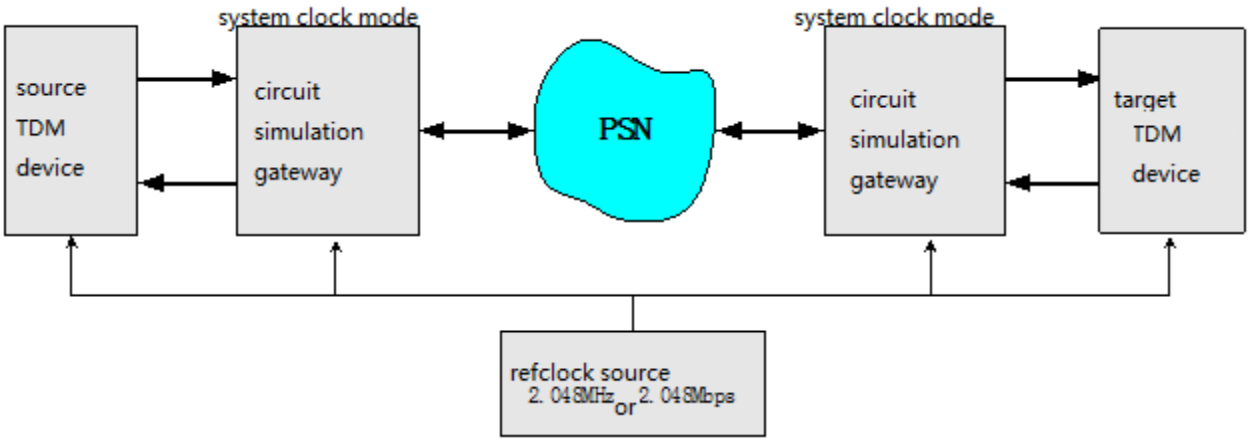



Differential clock recovery mode

### 1.5.3 System clock recovery mode

System clock mode: make one site's gateway as clock source of the whole system, all the other TDM equipment will abstract or follow the source clock, so as to realize synchronous frequency in the whole system. this mode can only be used in some certain application or testing.

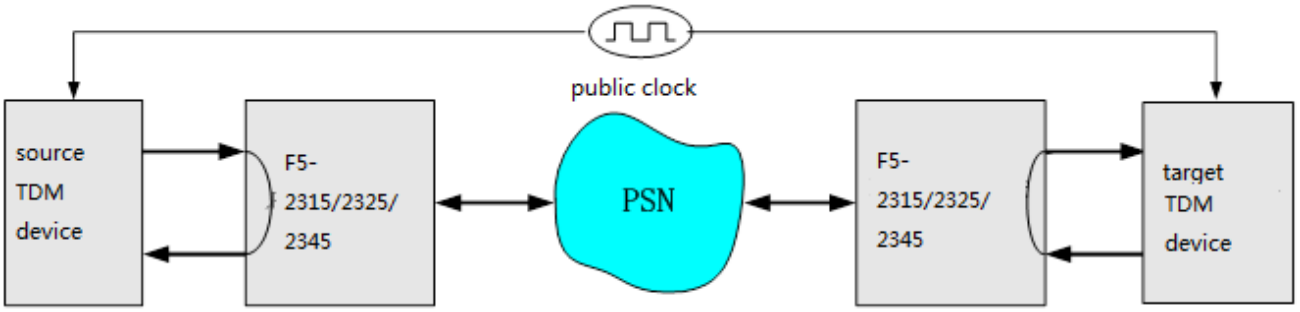
Like picture 1.5-3:




system clock mode

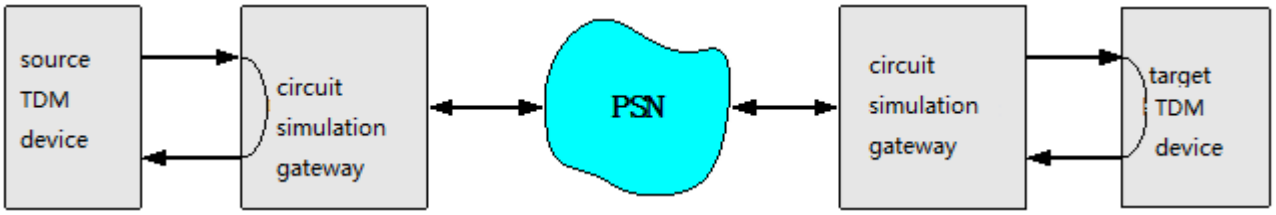
### 1.5.4 Loopback clock recovery mode

When all the equipment in TDM network has the same one clock source, circuit simulation gateway two ends can all be set to be E1 loopback clock recovery mode. The E1 clock recovered from two ends' E1 loopback mode has lowest jitter, highest clock assurance and best stability. Moreover, the recovered clock doesn't impacted by PSN network circumstance.




Pic.1.5-4 two ends E1 loop clock recovery mode

Nevertheless, in most scenario, equipment's in TDM network don't use the same one clock source, Circuit simulation gateway's one side uses E1 loop clock recovery mode, while the other side uses E1 self-adapt clock recovery mode. But target TDM equipment's transmitting clock must be from clock recovered by receiver side. As picture 1.5-5, when use E1 loop clock recover mode, E1 clock recovered from one side's gateway has the least jitter, the highest clock precision and the best stability. Additionally, recovery clock isn't impacted by PSB network environment.




Pic. 1.5-5 one side E1 loop clock recovery mode and the other side self-adapt mode

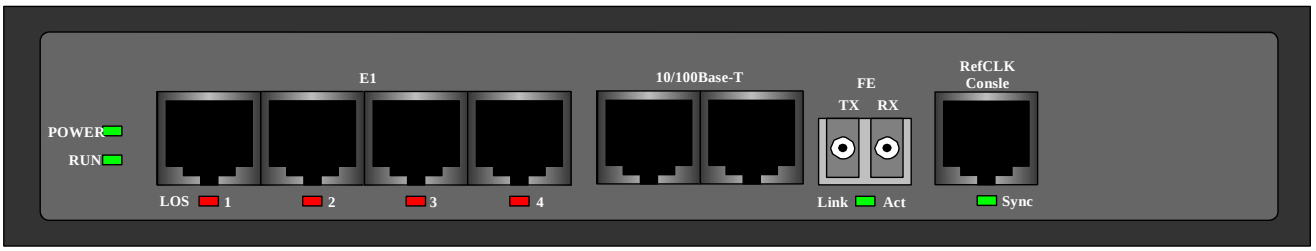
It's important to choose appropriate clock mode to ensure service quality. In most uses, customers can set both sides to be self-adapt mode.

# 2 System Construction

## 2.1 Panel Description

### 2.1.1 Panel Description

F5-2315/2325/2345 has its power and switch on back panel; E1 port, Ethernet port, status LED, reference clock input port on front panel. F5-2345 ’s front panel is as follows:




Pic. 2.1-1 F5-2315/2325/2345 front panel


Pic. 2.1-2 F5-2315/2325/2345 back panel

### 2.1.2 LED introduce

F5-2315/2325/2345 device front panel LED introduction refers to table 2.4-1 and 2.4-2.

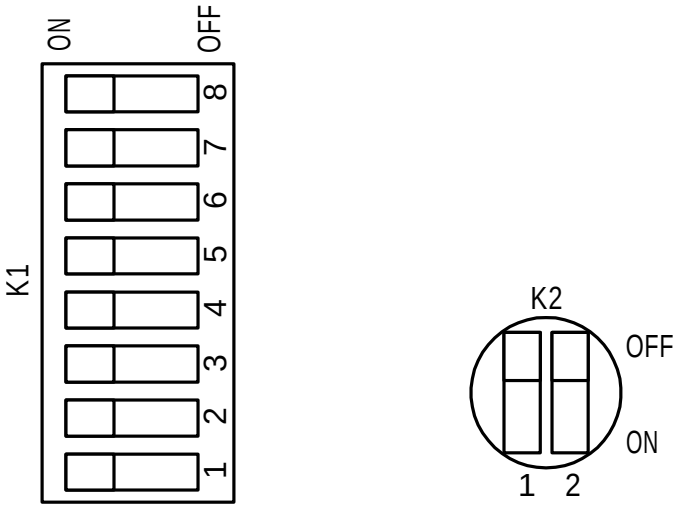
Table 2.1-1 F5-2315/2325/2345 device LED introduction

| Sign | color | quantity | meaning | remarks |
|---|---|---|---|---|
| POWER | green | 1 | Power status:<br>On: device works normally | |

| | | | | |
|---|---|---|---|---|
| | | | Off: device defective or power not connected | |
| RUN | green | 1 | Device running status:<br>Flash: device runs normally.<br>On or off: device doesn't run normally. | |
| Link/Act | green | 1 | Ethernet optic port connection status:<br>On: already connected with remote optic port.<br>Off: not connect with remote optic port.<br>Flash: data inputted. | Ethernet optic port LED light |
| SYNC | red | 1 | Reference clock input status:<br>On: no reference clock input<br>Off: there is reference clock input | |
| LOS<br>1-4E1 | red | 4 | E1 port LOS, AIS, LOF, CRC alarm indicator:<br>On: there is LOS or AIS alarm on port<br>Off: no alarm on port<br>Flash: there is LOF or CRC alarm on port | Each E1 port correspond to one LED light, to switch alarm indication by DIP switch. |

### 2.1.3 DIP switch control

F5-2315/2325/2345's bottom panel has one 8 bits and another 2 bits DIP switch. DIP definition is as below table, DIP switch's serial number and "ON" side definition refers to signs on DIP switch.




Pic. 2.1-3 DIP switch definition

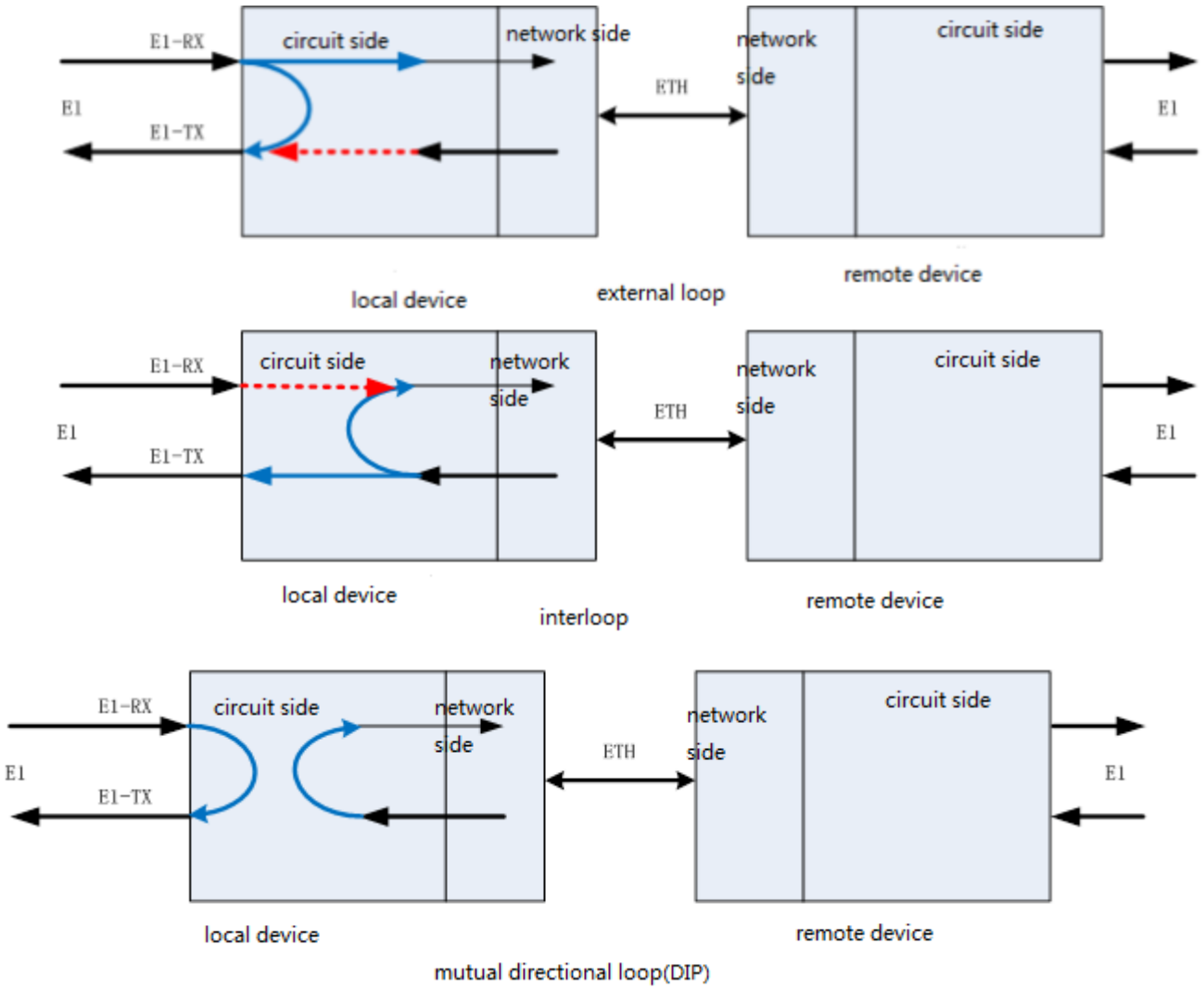
Table 2.1-2 K1 DIP switch function and meaning

| K1 | name | description |
|---|---|---|
| 1 | ArmSEL | Alarm indicator choose, ON: LOS or LOF(flash), OFF: AIS or CRC(flash) |
| 2 | RE/LO | Local and remote alarm indicator choose, ON: display local, OFFL display remote. |
| 3 | E1LOOP | E1 loop control, ON: loop disable, OFF: loop enable. |
| 4 | MIILOOP | MII loop control, ON: loop disable, OFF: loop enable. |
| 5 ~ 8 | 75/120Ω | Separately correspond to the 4th to 1st channel E1 port impedance choose, ON: 75Ω, OFF:120Ω. |

Table 2.4-3 K2 DIP switch function and meaning

| K2 | name | Description |
|---|---|---|
| 1 | Reset | Recover factory setting(needs reset), OFF: recover factory setting, ON: user configuration. |
| 2 | 75/120Ω | Reference clock port impedance chooses, ON: 75Ω, OFF: 120Ω. |

Local loop includes E1 side's loop, network side's loop and mutual directional loop (F5-2315/2325/2345 series product currently only support E1 side's loop) which is set by DIP switch. Mutual directional loop has top priority, as below pictures:

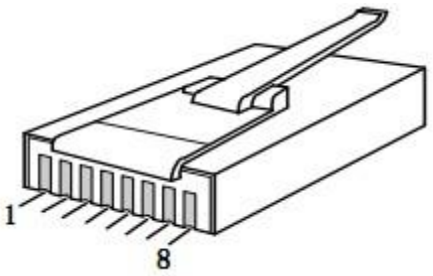



Pic. 2.1-4 local loop

### 2.1.4 E1 port

F5-2315/2325/2345 provides 1/2/4 channels E1 ports, 120Ω balance and 75Ω unbalance connector.

120Ω balance connector uses RJ45, each RJ45 is correspond to 1 channel E1. RJ45 connector and PIN definition is as picture 2.4-5 .



Pic. 2.1-5 RJ45 pin serial

When use 120Ω E1 port, the cable can be made according to table 2.4-3. Mind the twisted pair connection, otherwise will cause disturb.

Table 2.1-4 RJ45 corresponds to E1 cable table

| RJ45 PIN | E1 cable | Twisted pair | CAT-5 made color |
|---|---|---|---|
| 1 | OUT（1）+ | Match pair | Orange |
| 2 | OUT（1）- | | Orange and white |
| 4 | IN（2）+ | Match pair | blue |
| 5 | IN（2）- | | Blue and white |
| 3、6、7、8 | NC | | |

### 2.1.5 Ethernet port

F5-2315/2325/2345 gateway front panel provides two 100M Ethernet copper ports and one 100M Ethernet optic port. Ethernet embeds 2 layer switch function, supports VLAN division based on 802.1q or 802.1ad Q in Q , and 802.1p VLAN priority division. Three Ethernet ports can realize Ethernet switch function, any of them can be upload data port or local data port. User can link any Ethernet port for management.

Ethernet copper port uses RJ45 jet, RJ45 port's cable definition refers to table 2.4-4. Ethernet optic port uses LC connector, applies different SFP modules according to transmission distance needs.

10/100Base-T

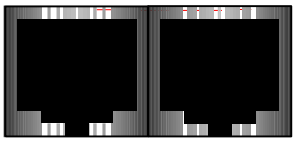


Table 2.1-7 Ethernet copper port

Table 2.1-5 RJ45 Ethernet port definition

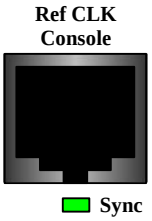
| Pin | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| definition | TxD+ | TxD- | RxD+ | NC | NC | RxD- | NC | NC |

**Notice**

This product's Ethernet copper port has HP auto-MDIX function, can auto detect Ethernet cable's Tx/Rx serial and auto-adapt. So, no matter the connecting Ethernet port is MDI or MDI-X port, no matter the Ethernet cable is 568B or 568A standard, aka cross/non-cross, the connection is OK.

### 2.1.6 Reference clock input and console port

F5-2315/2325/2345 device front panel provides 1 channel reference clock input and 1 channel console(RS232) port, definition is as follows:




Pic. 2.1-8 reference clock input and console port

Table 2.1-5 reference clock input RJ45 PIN definition

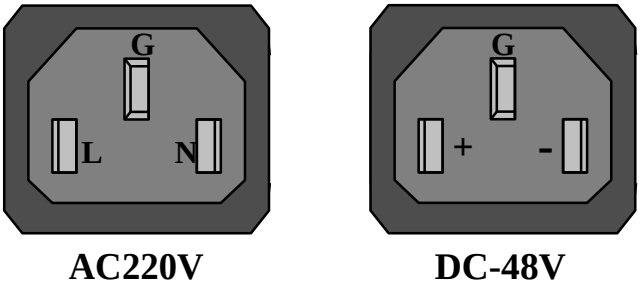
| PIN | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| definition | x | x | TX | CLKIN+ | CLKIN- | RX | GND | x |

CLKIN+ and CLKIN- is one pair reference clock input signal cable.

Console port definition: TX: device transmit, RX: device receiver, GND: ground.

### 2.1.7 Power input

L F5-2315/2325/2345 device black panel provides 1 power socket and 1 switch, supporting AC220Vand DC-48V. User please follow below diagram to connect, to avoid device damage. See picture 2.4-9.




Pic. 2.1-7 power supply

# 3 Main technical parameter

## 3.1 E1 port parameter

- Point to point one-way addition process time delay (in minimum time delay setting)≤1.2ms
- Output frequency stability (self-adapt timing, after stabilize) ≤ 50ppb
- output jitter (self-adapt timing) ≤ 0.03UI

## 3.2 Ethernet port parameter

- Support Ethernet speed rate limit, range is 32Kbps~100Mbps, minimum set unit is 32kbps.